Amendments to the Claims

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims

1-10. (Canceled)

11. (Currently Amended) A signal line driver circuit comprising:

a shift register;

a latch circuit, electrically connected to the shift register, comprising a plurality of pairs of current source circuits, ~~sources,~~ wherein each of the plurality of pairs of current source circuits ~~sources~~ is configured to receive a set signal and a signal current, and to control an output current value depending on a value of the signal current; and

a changing over circuit electrically connected to the plurality of pairs of current source circuits ~~sources~~ and a plurality of signal lines,

wherein the changing over circuit is configured to select one pair of current source circuits ~~sources~~ from the plurality of pairs of current source circuits~~sources~~ for electrically connecting to each of the plurality of signal lines, and

wherein the shift register is configured to output the set signal.

12. (Currently Amended) A signal line driver circuit comprising:

a shift register;

a latch circuit, electrically connected to the shift register, comprising:

a plurality of pairs of current source circuits~~sources~~, wherein each of the plurality of pairs of current source circuits ~~sources~~ is configured to receive a set signal and a signal current, and to control an output current value depending on a value of the signal current;

a first switch provided between the shift register and each of the plurality of pairs of current source circuits; ~~sources;~~ and

a second switch, and

a changing over circuit electrically connected between the plurality of pairs of current source circuits ~~sources through the second switch~~ and a plurality of signal lines,

wherein the changing over circuit is electrically connected to a particular pair of current source circuits through the second switch,

wherein the changing over circuit is configured to select one pair of current source circuits~~sources~~ from the plurality of pairs of current source circuits ~~sources~~ for electrically connecting to each of the plurality of signal lines,

wherein the shift register is configured to output the set signal, and

wherein the first and second switches are configured to be controlled by a latch pulse.

13-80. (Canceled)

81. (Previously Presented) A signal line driver circuit comprising:

a plurality of current source circuits, wherein each of the plurality of current source circuits is configured to be supplied with a first current and to supply a second current, and wherein a value of the second current depends on a value of the first current;

a plurality of signal lines; and

a selector circuit electrically connected between the plurality of current source circuits and the plurality of signal lines, wherein the selector circuit is configured to select one of the plurality of signal lines to which the second current is supplied.

82. (Currently Amended) The signal line driver circuit according to claim 11 wherein each of the current source circuits ~~sources~~ includes at least one switch and at least one transistor having a gate, with the switch being connected to control a voltage applied to the gate of the transistor.

83. (Currently Amended) The signal line driver circuit according to claim 12 wherein each of the current source circuits ~~sources~~ includes at least one switch and at least one transistor

having a gate, with the switch being connected to control a voltage applied to the gate of the transistor.

84. (Previously Presented) The signal line driver circuit according to claim 81 wherein each of the current source circuits includes at least one switch and at least one transistor having a gate, with the switch being connected to control a voltage applied to the gate of the transistor.

85. (New) The signal line driver circuit according to claim 11 wherein:

each of the current source circuits includes at least one capacitor and at least one transistor, and operates in a set mode or an output mode depending on a value of the set signal received by the current source circuit;

in the set mode, the capacitor is charged to a potential depending on the value of the signal current; and

in the output mode, the output current value depends on the potential to which the capacitor is charged.

86. (New) The signal line driver circuit according to claim 85 wherein:

when a first current source circuit of a pair of current source circuits is operating in the set mode, a second current source circuit of the pair of current source circuits is operating in the output mode; and

when the second current source circuit of the pair of current source circuits is operating in the set mode, the second current source circuit of the pair of current source circuits is operating in the output mode.

87. (New) The signal line driver circuit according to claim 12 wherein:

each of the current source circuits includes at least one capacitor and at least one transistor, and operates in a set mode or an output mode depending on a value of the set signal received by the current source circuit;

in the set mode, the capacitor is charged to a potential depending on the value of the signal current; and

in the output mode, the output current value depends on the potential to which the capacitor is charged.

88. (New) The signal line driver circuit according to claim 87 wherein:

when a first current source circuit of a pair of current source circuits is operating in the set mode, a second current source circuit of the pair of current source circuits is operating in the output mode; and

when the second current source circuit of the pair of current source circuits is operating in the set mode, the second current source circuit of the pair of current source circuits is operating in the output mode.

89. (New) The signal line driver circuit according to claim 12, further comprising a third switch connected between the particular pair of current source circuits and the signal current, wherein the second and third switches are controlled such that, when the second switch is configured to select a first current source circuit of the particular pair of current source circuits, the third switch is configured to select a second current source circuit of the particular pair of current source circuits, and, when the second switch is configured to select the second current source circuit of the particular pair of current source circuits, the third switch is configured to select the first current source circuit of the particular pair of current source circuits.

90. (New) The signal line driver circuit according to claim 81 wherein:

each of the current source circuits includes at least one capacitor and at least one transistor, and operates in a set mode or an output mode depending on a value of the set signal received by the current source circuit;

in the set mode, the capacitor is charged to a potential depending on the value of the signal current; and

in the output mode, the output current value depends on the potential to which the capacitor is charged.

91. (New) The signal line driver circuit according to claim 90 wherein:

when a first current source circuit of a pair of current source circuits is operating in the set mode, a second current source circuit of the pair of current source circuits is operating in the output mode; and

when the second current source circuit of the pair of current source circuits is operating in the set mode, the second current source circuit of the pair of current source circuits is operating in the output mode.